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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,266	03/31/2004	Douglas Holberg	CYGL-26,655	9833

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/816,266	HOLBERG ET AL.
	Examiner	Art Unit
	Hiep Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 01-21-06. Applicant's arguments with respect to 112, 2nd paragraph and reference Shin (US Pat. 6,107,871) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under 112, 2nd paragraph and Shin. However, the rejection changes slightly for clarification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation " a first clock rate" in claim 1 is indefinite because it is not clear what it is meant by. As understood by the examiner, the clock rate is expressed in cycles per second, not the duty cycle of the clock. (see attached document). The sampling of the input is done by clock Ø1. It is not clear if the "a first clock rate" is the time clock Ø1 is high. The recitation " dumping charge from the input sampling capacitor to the non inverting input of the amplifier at a second time and at the first clock rate" on lines 6-7 is indefinite because it is misdescriptive. Figure 2 of the present application shows that signal Ø2 controls switches 110 and 118 to dump charge from the input sampling capacitor (C1) to the non inverting input of the amplifier when the second clock Ø2 is at high level. The " second time of the first clock rate" Ø1 does not turn switches 110 and 118 on as recited. The recitation "sampling a reference voltage onto a feedback sampling capacitor at substantially the first clock rate" on lines 8-9 is indefinite because it is

The feedback sampling capacitor (C2) samples the reference voltage (Vref) when switches (134) and 152 close with a "rate" (Θ1/D) and switch (152) closes at "rate" Ø1 (first rate). Thus, with the combination of these two "rates", sampling a reference voltage onto a feedback

sampling capacitor (C2) is not done at substantially the "first rate" (Ø1). Moreover, clock (Θ1/D) is not shown in the timing diagram, figure 2. Clear explanation is required.

Regarding claim 2, the recitation "the first clock rate" is indefinite because of the same reason raised above. The recitation "generating a second clock with a second stream of periodic pulses and shifted **in phase from** the first clock and **synchronous therewith**" on line 5-6 is indefinite because it is misdescriptive. Figure 2 of the present application shows that the first and second clocks Ø1 and Ø2 are **not in phase.** They are **non-overlapped clocks** thus, they are **not in synchronism**. In fact, clock Ø1 and Ø2 are 180 degrees out of phase. If clock (Ø1) is high, clock (Ø2) is low. Clear explanation is required.

Regarding claim 9, the recitations " first clock rate", "second clock rate" in the claim, "a second time and at the first clock rate", "the first clock rate and at the first clock rate" on line 8, "the first clock rate" on line 10, "a second rate", "the first clock rate" on line 12, "the second clock rate" and the "first clock rate" on line 16 have the same 112,2[nd] problem raised above.

The recitation "an input sampling... at a second time and at the first clock rate" on lines 5-8 is indefinite because it is misdescriptive. Sampling the input voltage and dumping charge are controlled by different clock signals Ø1 and Ø2 having different duty cycles, thus they are not at the "same clock rate".

The recitation "a first dump circuit ...a second time and at a first clock rate" on lines 7-8 is indefinite because it is misdescriptive. Figure 1 of the present application shows that the input voltage (Vin) is dumped the charge from capacitor (C1) to the non inverting input with clock Ø2 that is different from clock Ø1.

The recitation " a gain control input for receiving a gain control input controller for controlling the amount of time that charge is dump from said feedback sampling capacitor relative to the amount of time that charge is being dumped from said input sampling capacitor" on lines 13-15 is indefinite because it is not clear what it is meant by. This "gain controller" is not seen in the drawing and it is not disclosed in the specification. It is not clear how the gain controller can control the "amount of time" and what the recitation "varying the second rate relative to the first rate changes the gain of delta-signal converter" is meant by.

Regarding claim 10, the recitations "the first clock rate" and "generating a second stream of periodic pulses and **shifted in phase** from said **first clock** and **synchronous therewith**" are indefinite because it is not clear what the recitations "the first clock rate", "shift in phase" and "synchronous therewith" are meant by. Figure 2 of the present application shows that clocks Ø1 and Ø2 are **non-overlapped clocks** and are 180 degrees out of phase. If clock Ø1 is high, clock Ø2 is low. Therefore, clocks Ø1 and Ø2 are not **in phase and in synchronism**. Clear explanation is required.

Claims 3-8 and 11-16 are indefinite because of the technical deficiencies of claims 1 and 6.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (USP. 6,107,871).

Regarding claim 1, figurer 6 or 7 of Shin shows a method for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output, comprising the steps of:

sampling an input voltage (Vinp) at a "first lock rate" (Ø1) having a first duty cycle onto an input sampling capacitor (C/4);

dumping charge from the input sampling capacitor (C/4) to the non-inverting input of the amplifier at a second time (Ø2) and at a "second clock rate" (second duty cycle);

sampling a reference voltage (Vinp) onto a input sampling capacitor (C/4) at substantially the "first clock rate" (Ø1);

dumping charge stored on the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier at a "second clock rate" (Ø2) different than the first rate; and

controlling the amount of time by varying the duty cycle of signal (Ø2) that charge is dumped from the feedback sampling capacitor (C/4) to be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor (note that the dumping of the charges onto the negative feedback of the amplifier is performed with the same clock signal (Ø2);

wherein varying the "second clock rate" (Ø2) relative to the "first clock rate" changes the gain of delta-sigma converter.

Regarding claims 2 and 3, the steps of sampling an input voltage at the "first clock rate" (Ø1) onto an input sampling capacitor (C/4) and dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprise:

generating a first clock (Ø1) with a first stream of periodic pulses at the "first clock rate" or first duty cycle;

generating a second clock (Ø2) with a second stream of periodic pulses;

sampling the input voltage (Vinp) onto the input sampling capacitor (C/4) during the time that the first stream of pulses (Ø1) are high; and

dumping charge from the input sampling capacitor (C/4) to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high. Pulses (Ø1) and (Ø2) are non-overlapping

Regarding claim 4, the step of sampling the input voltage on the input sampling capacitor comprises the steps of connecting one plate of the input sampling capacitor (C/4) to the input voltage (Vinp) and the other plate of the input sampling capacitor to ground during the time that the first stream of pulses (Ø1) are high; and

the step of dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the input sampling capacitor (C/4) to ground and the other plate of the input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high.

Regarding claim 5, the steps of sampling the reference voltage onto the feedback sampling capacitor and dumping charge stored on the feedback sampling capacitor to the non- inverting input of the amplifier comprises the steps of:

sampling the reference voltage (Vinn) onto the feedback sampling capacitor (C/4) during the time that the first stream of pulses (Ø1) are high; and

dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different rate than the step of sampling the reference voltage onto the feedback sampling capacitor.

Regarding claim 6, the step of sampling the reference voltage on the feedback sampling capacitor comprises the steps of connecting one plate of the feedback sampling capacitor (C/4) to the reference voltage (Vinn) and the other plate of the feedback sampling capacitor to ground during the time that the first stream of pulses (Ø1) are high; and the step of dumping charge from the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the feedback sampling capacitor to ground and the other plate of the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different rate than the step of sampling the reference voltage onto a feedback sampling capacitor. Note that signals (Ø1) and (Ø2) have different duty cycles.

Regarding claim 7, the step of dumping charge stored on the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses are high, and the number of the pulses in the second stream of pulses during which the step of dumping charge stored on the feedback sampling capacitor to the non- inverting input of the amplifier is less than all of the pulses in the second stream of pulses.

Regarding claim 8, the step of generating a control signal in a control circuit, not shown, that generates and regulating signals (Ø1) and (Ø2), that selects the ones of the pulses in the second stream of pulses during which charge stored on the feedback sampling capacitor (C/4) is dumped to the non-inverting input of the amplifier with clock (Ø2),.

Regarding claim 9, figure 6 of Shin shows a gain control circuitry for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output comprising:

an input sampling circuit (SW1, SW4) for sampling an input voltage at a "first clock rate" (duty cycle) (Ø1) onto an input sampling capacitor (C/4);

a first dump circuit (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier at a second duty cycle of clock (Ø2);

a feedback sampling circuit (SW13, SW16) for sampling a reference voltage (Vinn) onto a feedback sampling capacitor at substantially the "first clock rate" (duty cycle) (Ø1);

a second dump circuit (SW14, SW15) for dumping charge stored on said feedback sampling capacitor (C/4) to the non-inverting input of the amplifier at a "second clock rate" (duty cycle) (Ø2) different than the first duty cycle;

a gain controller, not shown, for controlling the amount of time (the duty cycle of Ø2) that charge is dumped from said feedback sampling capacitor (C/4) to be substantially equal to the amount of time (Ø2) that charge is being dumped from said input sampling capacitor;

wherein varying the second rate relative to the first rate changes the gain of delta-sigma converter.

Regarding claim 10, the first dump circuit comprises:

a first clock for generating a first stream of periodic pulses (Ø1) at the "first clock rate";

a second clock for generating a second stream of periodic pulses (Ø2);

first switching circuitry (SW1, SW4) for sampling the input voltage onto the non-inverting input of the amplifier during the time that the first stream of pulses (Ø1) are high; and

second switching circuitry (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high.

Regarding claim 11, the first stream of periodic pulses and said second stream of periodic pulses are non overlapping (Fig. 8).

Regarding claim 12, the first switching circuitry includes

a first switch (SW1) for connecting one plate of said input sampling capacitor to the input voltage, and

a second switch SW4) for connecting the other plate of said input sampling capacitor to ground during the time that the first stream of pulses are high; and

said second switching circuitry includes:

a third switch (SW3) for connecting the one plate of said input sampling capacitor to ground, and

a fourth switch (SW2) for connecting the other plate of said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) is high.

Regarding claim 13, the second sampling circuit and said second dump circuit comprise:

third switching circuitry (SW13, WS16) for sampling said reference voltage (Vinn) onto the non-inverting input of the amplifier during the time that the first stream of pulses (Ø1) are high; and

second switching circuitry (SW14, SW15) for dumping charge from said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different rate than the rate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 14, the third switching circuitry includes:

a fifth switch (SW13) for connecting one plate of said feedback sampling capacitor to the reference voltage (VINN), and

a sixth switch (SW16) for connecting the other plate of said feedback sampling capacitor to ground during the time that the first stream of pulses are high; and said fourth switching circuitry includes:

a seventh switch (SW15) for connecting the one plate of said feedback sampling capacitor to ground, and

an eighth switch (SW14) for connecting the other plate of said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second

stream of pulses (Ø2) are high and at a different rate than the rate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 15, the dumping of charge stored on said feedback sampling capacitor to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses (Ø2), and the number of the pulses in the second stream of pulses during which dumping of charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier is <u>less</u> than all of the pulses in the second stream of pulses (Fig. 8).

Regarding claim 16, the control signal (not shown) that selects the ones of the pulses in the second stream of pulses (Ø2) during which charge stored on the feedback sampling capacitor is dumped to the non-inverting input of the amplifier.

Response to Arguments

In the Remarks, page 8, the Applicant explains that the "first rate" and "second rate" refer to clock rates. This is not true because by definition, the <u>clock rate</u> is the number of cycles of the clock signal (see attached document). According to figure 2 of the present application, the high/ low levels of the clock signals (Θ1) and (Θ2) control the operation of the switches, not the <u>clock rate</u> i.e., the number of cycles of the clock signal. Moreover, figure 2 of the present application shows that clocks (Θ1) and (Θ2) are two non-overlapped clocks. When clock (Θ1) is high, clock (Θ2) is low or vice versa. Switches 106, 116 and 110, 118 are turned on/off at different times. <u>The on/off of these switches are not related to the rates i.e.,</u> the number of cycles of the clock signals. Assume that clock (Θ1) is high, clock (Θ2) is low switches 106 and 116 are turned on with the high level of the clock Θ1. At the time the level of clock (Θ1) is high, clock (Θ2) is low and switches 106 and 116 are turned off and switches 110, 118 are turned on to "dump" the charge stored in capacitor (C1) to the non-inverting input. <u>Therefore, the switches function with the **levels** of the clock signals, not the **rates** of the clocks</u>. Figure 2 shows that switch 134 and switch 152 are turned on when the level of clocks (Θ1) and (Θ1.D/) that are both at high level in order to sample the reference voltage Vref. In the second paragraph the Applicant argues that "the claims clearly state that these are

synchronous". Figure 2 shows that clocks ($\Theta1$) and ($\Theta2$) are two non-overlapped clocks and one of ordinary skill in the art understand that non-overlapped clocks are not synchronous clocks. If they are synchronous clocks, they switches will be turned on/off at the same time. Note that clocks ($\Theta1$) and ($\Theta2$) are not "shifted in phase" as claimed. Therefore, claims1, 2, 9 and 10 remain rejected under 112, 2^{nd} paragraph.

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
03-09-06

TUAN T. LAM
PRIMARY EXAMINER